Improved pulse-width modulation scheme for T-type multilevel inverter

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Abstract: In recent times, reduced switch count multilevel inverter (RSC-MLI) has become an emerging area of research in power electronic converters. To control these RSC-MLI topologies, various novel modulation schemes are reported. Multi-reference is one of such modulation scheme reported for various RSC topologies, such as T-type. However, the performance of this conventional scheme results in high total harmonic distortion (THD) in line voltages, when compared with the conventional level shifted pulse-width modulation scheme. This observation is clearly presented in this study and the reason for its degraded THD performance has been deeply discussed. To alleviate this problem, a modified multi-reference dual-carrier modulation technique with multiple references and two carriers is proposed. To implement this proposed modulation technique, an alternate carrier and modulation signals arrangement with multiple carriers and single reference is also presented. Finally, a comparative THD performance of the proposed and conventional modulation schemes is carried out on a five-level T-type MLI and obtained simulation results are validated experimentally.

1 Introduction

Multilevel inverters (MLIs) use the concept of addition of small multiple voltage levels and possess various advantages like reduction in dv/dt, electro-magnetic interference and total harmonic distortion (THD) [1, 2]. In literature, cascaded H-bridge (CHB), diode clamped and flying capacitor are the widely accepted classical MLI topologies, and are reported with various modulation strategies, such as sinusoidal pulse-width modulation (SPWM), selective harmonic elimination (SHE), third harmonic injection and space vector modulation (SVM) [3–8]. Among these conventional schemes, SPWM is very popular due to its easiness in implementation and is further classified into level shifted pulse-width modulation (LSPWM) and phase shifted pulse-width modulation (PSPWM) [9]. LSPWM is sub-classified into in phase disposition (IPD), opposite phase disposition (OPD) and alternate phase disposition (APD). It is well reported that LSPWM-IPD results in better line THD performance compared with LSPWM-OPD, LSPWM-APDand PSPWM [9].

In practice, MLIs are limited to lower levels, because of its increased switch count at higher levels. This increase in switch count not only turns the topology complex but also raises its overall cost. Form past two decades, there is an extreme exploration carried out to evolve newer topologies with reduced switch count (RSC). T-type is one of the recently reported RSC-MLI, which gathered much attention. T-type possesses most feasible and generalised configuration with 37.5% reduction in switch count compared with classical topologies [10–12]. Extreme reduction in switch count of RSC-MLI's created diversified effects on switching states such that, most popular conventional SPWM schemes are insufficient to implement them [13, 14]. In literature, few of such RSC configurations are reported with SHE and SVM methods. However, these schemes involve complex mathematical calculations, which turn more complicated at higher levels [23]. Recently, few RSC topologies are reported with multi-carrier modulation schemes involving logical expressions. However, these logical expressions are not generalised, and vary with variation in number of levels and topological arrangement [15]. A novel multi-reference modulation scheme for T-type MLI is reported, and a seven-level T-type with multi-reference modulation for grid connected systems is reported in [16, 17]. This scheme is accepted widely, due to its generalised nature which can be applicable to any RSC configuration [18–21]. However, this scheme suffers from high THD in line voltages when compared with the conventional LSPWM scheme. In [22], a phase shifted multi-reference modulation scheme is reported for cascaded T-type topologies. In this method, the number of carriers is equal to the number of modules that are connected in cascade and moreover, when considering a single module its performance is identical to a conventional multi-reference modulation scheme.

From the keen literature review of various multi-reference and multi-carrier modulation schemes reported for various RSC-MLI topologies, it is observed that, most of these schemes either result in high THD in line voltages or suffers from generalisation of switching scheme at higher levels. This observation is clearly discussed in this paper and simple generalised modulation schemes are proposed, which obtain satisfactory line voltage THD performance on any RSC-MLI topology.

The structure of this paper is as follows. In Section 2, performance of conventional multi-reference modulation scheme on a five-level T-type MLI is discussed and the reason for its poor THD performance is analysed. In Section 3, modifications in the conventional multi-reference modulation scheme to improve its THD performance are suggested and a modified multi-reference dual-carrier modulation scheme is proposed. In addition, to implement the proposed scheme an alternative carrier and modulating signal arrangement is presented and generalisation of this scheme to higher levels is discussed with the help of a flowchart. Performance of the proposed scheme is investigated on a five-level T-type topology and their superior harmonic performance over conventional multi-reference modulation can be observed. Section 4 presents experimental results of the proposed and conventional modulation schemes on a five-level T-type MLI. Obtained simulation results are validated experimentally with dSPACE-1104 R&D control board. Finally, a comparative performance of the proposed and conventional modulation schemes, for a five-level MLI, at various modulation indices is carried out.
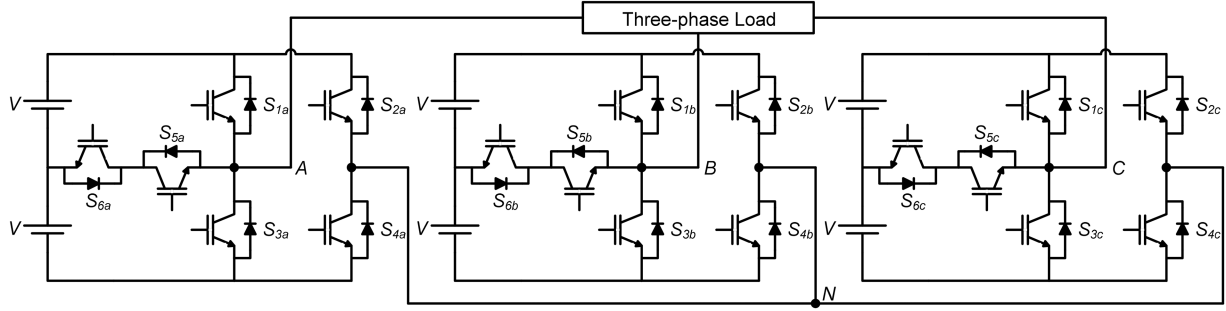
Fig. 1 *Five-level T-type topology*

Table 1 Operating switches to obtain respective voltage levels in each phase

Switches in conduction	Voltage level
S_5 and S_4	V
S_1 and S_4	$2V$
(S_1 and S_2) or (S_3 and S_4)	0
S_6 and S_2	$-V$
S_3 and S_2	$-2V$

2 T-type configuration and multi-reference modulation scheme

2.1 T-type configuration

T-type topology is the congregation of bidirectional and unidirectional switches. To obtain five levels in phase voltage, four unidirectional switches (S_1, S_2, S_3 and S_4), one bidirectional switch and two dc sources are required per phase as shown in Fig. 1. Considered bidirectional switch is represented with two back-to-back connected unidirectional switches (S_5 and S_6). The four unidirectional switches form an H-bridge and the isolated dc supplies are connected to H-bridge through the bidirectional switch. As the level increases, requirement of bidirectional switches and dc sources increases, but the switches in the H-bridge remains unaltered.

To obtain 'n' levels in phase voltage and '$2n-1$' levels in line, '$4+(n-3)$' switches are required per phase. Here, four indicate number of switches in H-bridge and '$n-3$' indicate additional unidirectional switches required.

2.1.1 Operation of the T-type MLI for five levels in phase: To obtain five levels in phase voltage, i.e. $2V$, V, 0, $-V$ and $-2V$, two dc sources (of each V volts) in each phase are required. In every phase, switching $S_4 - S_2$ and $S_1 - S_3$ obtains $2V$, $-2V$ levels, respectively. Similarly, switching $S_5 - S_4$ and $S_6 - S_3$ obtains $+V$ and $-V$ levels, respectively. Switching states to obtain desired voltage levels per phase are shown in Table 1.

2.2 Conventional multi-reference modulation – performance analysis

Conventional multi-reference modulation involves single carrier and $(n-1)/2$ shifted dc references to obtain 'n' levels in phase voltage [16]. In literature, this scheme is well reported for T-type topologies.

2.2.1 Observation: Performance analysis of conventional multi-reference scheme on a five-level T-type topology with 2 kW, 0.9 pf RL load is carried out, at 1500 Hz carrier frequency (f_c). Obtained phase voltage, line voltage and load currents are shown in Fig. 2a with their respective harmonic spectra in Fig. 2b.

From the harmonic spectra shown in Fig. 2b, the following conclusions can be drawn.

i. Amplitude of harmonic component at integer multiples of carrier frequency is zero.

ii. Odd order harmonics appear in the side band centred at integer multiples of carrier frequency.

Harmonic performance of conventional multi-reference modulation is compared with most popular LSPWM (IPD) modulation on a five-level CHB. Comparative line THD performance of both the schemes for various amplitude modulation indices (m_a) is carried out and is observed that conventional multi-reference modulation results in high THD in line voltages compared with LSPWM modulation. This observation is clearly presented in Fig. 2c.

2.2.2 Reason analysis: Reason for poor THD performance of conventional multi-reference scheme can be understood, by referring to Fig. 3. Position of references and carrier for obtaining five levels in phase voltage is provided in Fig. 3a, where Reference$_1$ is the modulus of modulating signal and Reference$_2$ is obtained by shifting Reference$_1$ by its carrier peak. From Fig. 3b, it can be stated that referring a unipolar carrier with respect to the modified (unipolar) modulating signal (Reference$_1$) is similar to referring a unipolar carrier to the positive half, and its mirror image to the negative half of the modulating signal, respectively. The position of carrier and its mirror image with respect to the modulating signal is shown in Fig. 3b, and resembles the position of carriers in LSPWM-OPD scheme, i.e. is shown in Fig. 3c. Careful examination of Figs. 3b and c verifies that position of carrier in multi-reference modulation and LSPWM-OPD are identical. Further this can be confirmed by comparing phase and line harmonic spectra of both these conventional schemes.

Harmonic spectra of phase and line voltages of LSPWM-OPD for a five-level CHB are depicted in Fig. 3d. Appearance of harmonic content in the side-bands centred at integer multiples of carrier frequency is reported in [9] and the same can be observed from Fig. 3d. It is to be noted that conclusions drawn from harmonic spectra of multi-reference modulation scheme (Section 2.2.1) are similar to side-band harmonics of LSPWM-OPD spectra. From this analysis, it can be concluded that inherent switching action of conventional multi-reference modulation is similar to LSPWM-OPD modulation.

In literature, LSPWM-OPD is not preferred for three-phase MLI, due to its poor line THD performance [9]. Therefore, by referring conventional multi-reference modulation scheme to any typical RSC configuration also results in poor line THD performance. Therefore, few modifications in carrier arrangements of conventional schemes are necessary to improve its harmonic performance [15, 16]. In this paper, a modified modulation scheme is proposed which serves as a better alternative to conventional modulation schemes.

3 Modulation schemes with improved THD performance

3.1 Multi-reference dual-carrier modulation scheme

One possible approach to improve THD performance of the conventional multi-reference modulation scheme is to change its carrier's position, such that its inherent switching scheme becomes similar to LSPWM-IPD. Therefore, a modified multi-reference dual-carrier modulation scheme is proposed by using two carriers
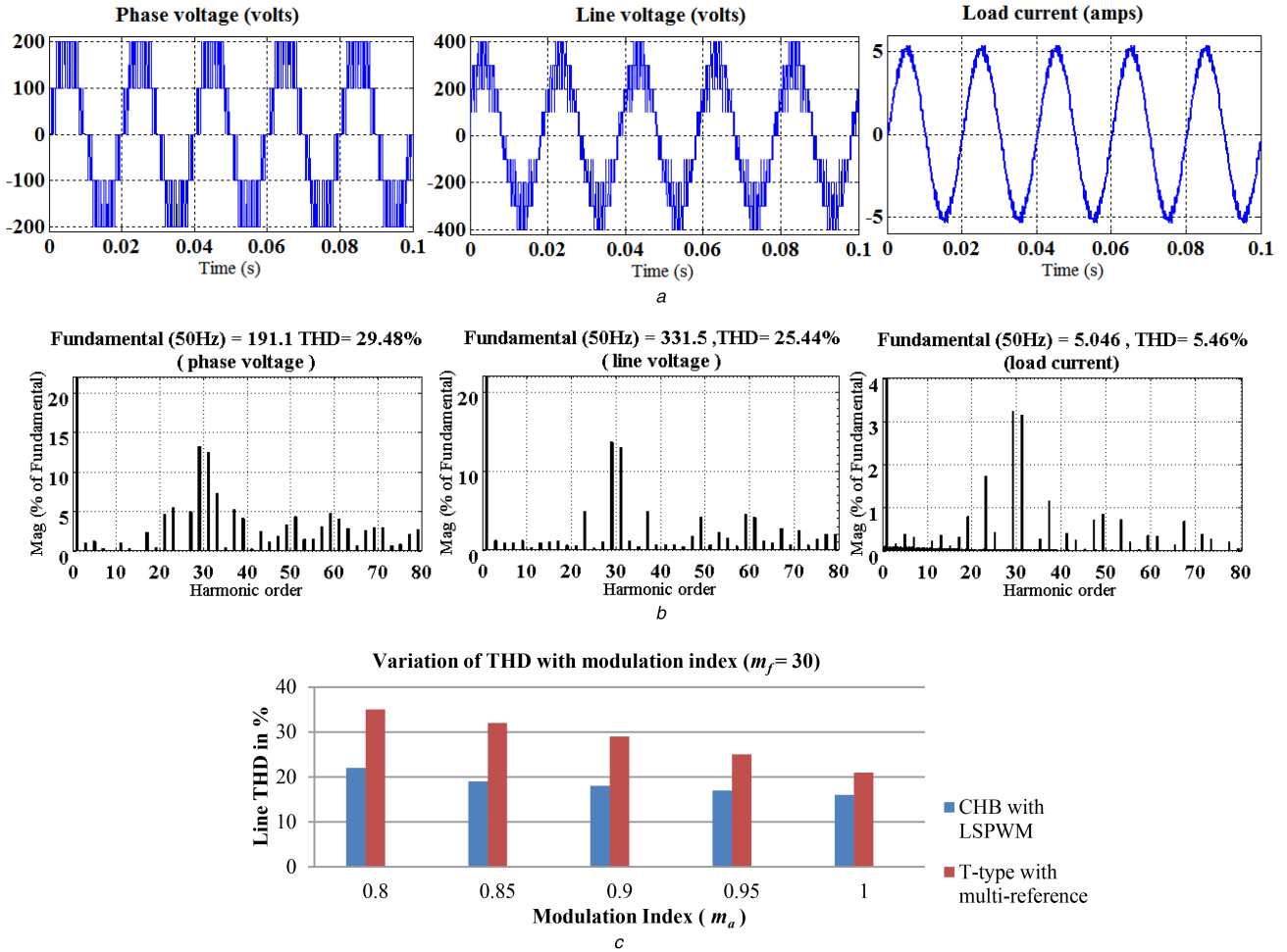
Fig. 2 *Performance analysis of multi-reference modulation scheme on five-level T-type configuration with $m_a = 0.95$ and $f_c = 1500$ Hz*
(a) Phase voltage, line voltage and load current, *(b)* Respective harmonic spectra, *(c)* Comparative harmonic performance of conventional multi-reference modulation scheme for five-level T-type MLI and LSPWM for five-level CHB

and '$(n−1)/2$' shifted dc references to obtain 'n' levels in phase voltage.

Arrangement of carriers and reference signals in the proposed scheme for a five-level MLI is shown in Fig. 4a. For a normalised modulating signal, carrier peak is decided by phase voltage levels in (1). Formula to calculate amplitude modulation index (m_a) is given in (2)

$$V_c = \frac{2}{n-1} \qquad (1)$$

$$m_a = \frac{V_m}{(n-1)V_C} \qquad (2)$$

V_m is the peak of the modulating signal, V_c is the peak of the carrier signal and n is the level in phase voltage.

The basic constraint of switching logic in modified multi-reference dual-carrier modulation is similar to the conventional multi-reference modulation. However, this conventional scheme involves only one carrier, i.e. Carrier$_1$, where the proposed scheme involves two carriers, i.e. Carrier$_1$ and Carrier$_2$. Both these carriers are of the same polarity and magnitude, but opposite in phase, as shown in Fig. 4a. Carrier$_1$ is used to obtain positive levels in phase voltage, by comparing with Reference$_1$ and Reference$_2$, for the positive half of the modulating signal. Similarly Carrier$_2$ is involved in obtaining negative voltage levels. The main intension behind using an additional carrier, i.e. Carrier$_2$, is to make its inherent switching action similar to LSPWM-IPD. This can be understood by referring to Fig. 4b, where the position of Carrier$_1$ and mirror image of Carrier$_2$, together resemble the position of the

carriers in LSPWM-IPD modulation scheme [9]. This statement can be further verified by observing harmonic performance of proposed multi-reference dual-carrier modulation.

Performance of the proposed scheme is investigated on a five-level T-type topology with 2 kW, 0.9 PF load. Obtained phase voltage, line voltage and load currents are shown in Fig. 4c. By its respective harmonic spectra shown in Fig. 4d, two observations can be drawn.

i. Amplitude of harmonic content at even multiples of carrier frequency is zero, but dominant harmonics appear at odd multiples of carrier frequency.
ii. Even-order harmonic components appear in the side-bands centred at odd multiples of carrier frequency. Similarly odd-order harmonic components appear in the side-bands centred at even multiples of carrier frequency.

From these observations it can be concluded that harmonic spectrum of the proposed scheme is identical to LSPWM-IPD reported in [9]. Hence, it verifies that modified multi-reference dual-carrier modulation inherent switching action is similar to LSPWM-IPD.

It is to be noted that, even though the phase voltage THD in Figs. 2b and 4d are almost same but the order of harmonics presented in these two spectra are different. However, there is a large difference in line voltage THD and this can be observed from Figs. 2b and 4d. This is because, in modified multi-reference dual-carrier modulation (and LSPWM-IPD) scheme, harmonics injected at odd multiples of m_f in consecutive phases are co-phasal in nature. Hence, they cancel out in line voltages, resulting in huge reduction in line voltage THD [9]. Therefore, in modified multi-reference dual-carrier modulation scheme the line voltage THD is
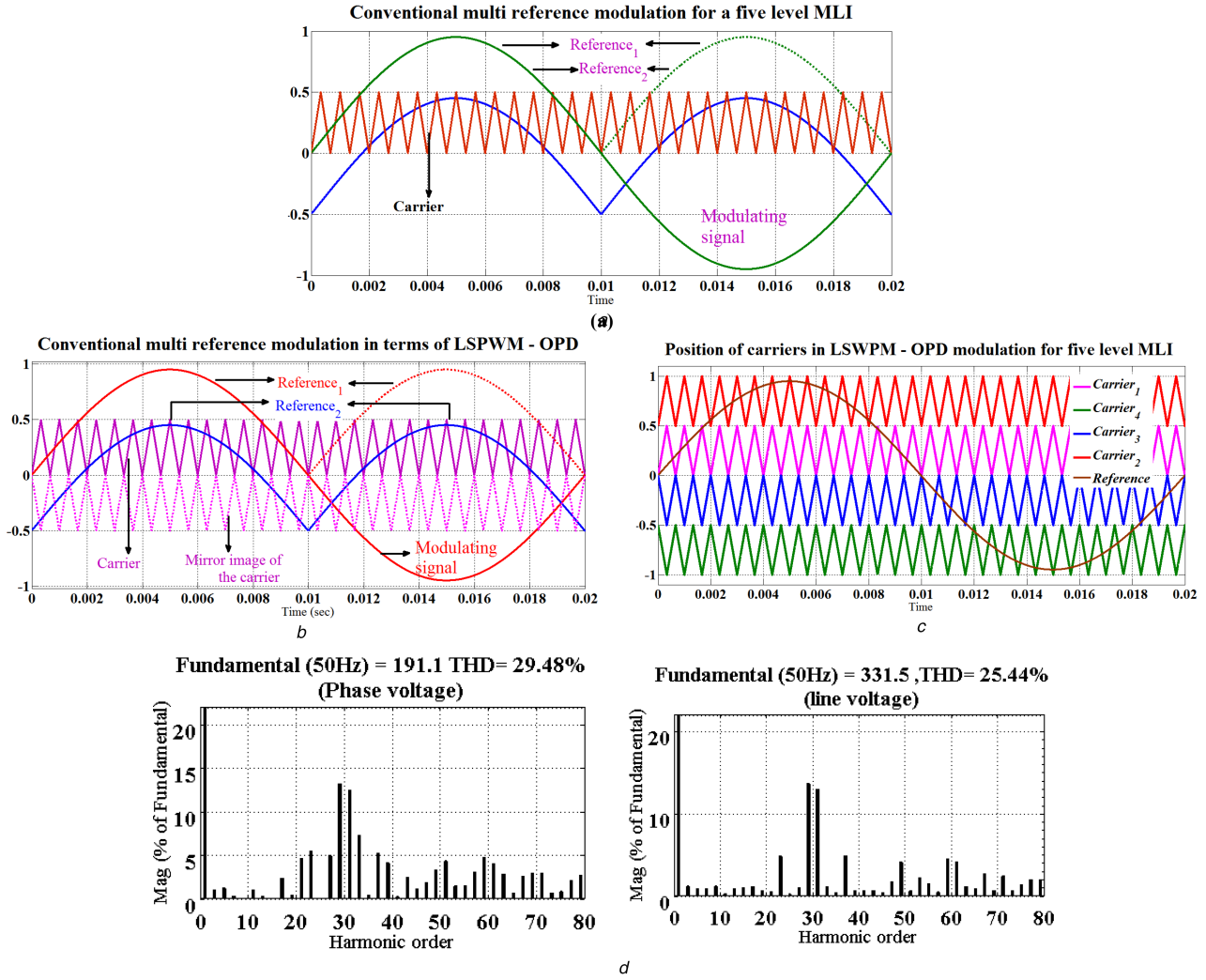
Fig. 3 *Comparison of LSPWM-OPD and multi-reference modulation scheme with $m_a = 0.95$ and $f_c = 1500$ Hz*

(a) Conventional multi-reference modulation scheme for a five-level T-type, *(b)* Comparison of position of carriers in multi-reference modulation in terms of LSPWM-OPD scheme,
(c) Position of carriers in LSPWM-OPD modulation scheme, *(d)* Phase and line harmonic spectra of LSPWM-OPD for a five-level CHB

less compared with conventional multi-reference modulation scheme. Further, the modified multi-reference dual-carrier modulation requires multiple shifted dc references which will increase its complexity for closed-loop applications. To alleviate this problem, an alternate carrier and modulation signals arrangement with multiple carriers and single reference is presented in below section.

3.2 Modified reduced carrier modulation scheme (alternate carrier and modulation signals arrangement of the proposed PWM scheme)

An alternate carrier and modulation signals arrangement with multiple carriers and single reference is presented in this section and is identical to the proposed modified multi-reference dual-carrier modulation scheme. This alternate method can be easily realisable on digital platforms. In this scheme, $(n-1)/2$ carriers are required to obtain 'n' levels in phase voltage. Carrier and modulation signal arrangement for a five-level converter is shown in Fig. 5a. If the modified reference (unipolar modulating signal) is less than Carrier$_1$ peak, then a voltage band of 0–V is obtained in phase voltage. If modified reference is greater than Carrier$_1$ peak, then V–2V band is obtained. Polarity of these voltage bands is decided by polarity of the modulating signal such that $+2V$, $+V$, 0, $-V$ and $-2V$ levels are obtained in phase voltage. The difference in carrier position for the positive and negative half of the modulating signal can be noticed from Fig. 5a. It should be noted that arrangement of each carrier in this modified scheme is the effective way of representing Carrier$_1$ and Carrier$_2$ of the proposed scheme

shown in Fig. 4a. This makes the inherent switching of this modified scheme identical to the proposed scheme (in Section 3.1). This can be further verified by observing the switching pattern of both these proposed and modified schemes on a five-level T-type topology, which is shown in Figs. 5b and c, respectively. These switching pulses are observed for 1500 Hz carrier frequency for $m_a = 0.95$.

The carrier and modulating signal arrangement for any number of levels and a flowchart to implement this method is shown in Fig. 6. Fig. 6a depicts carrier and modulating signal arrangement for any number of levels, where Carrier $_{1,2,3,4,5,\dots,(n-1)/2}$ are responsible for obtaining 0–V, V–2V, $2V$–3V… $(((n-1)/2)-1)V$ to $((n-1)/2)V$ bands, respectively. The maximum and minimum value of each carrier can be calculated from (3) and (4). The amplitude modulation index (m_a) and frequency modulation index (m_f) are defined in (5) and (6)

$$Carrier\ i_{\max} = \frac{2}{(n-1)}i \qquad (3)$$

$$Carrier\ i_{\min} = \frac{2}{(n-1)}(i-1) \qquad (4)$$

where i is the carrier number and n is the levels in phase voltage

$$m_a = \frac{2V_m}{(n-1)V_c} \qquad (5)$$

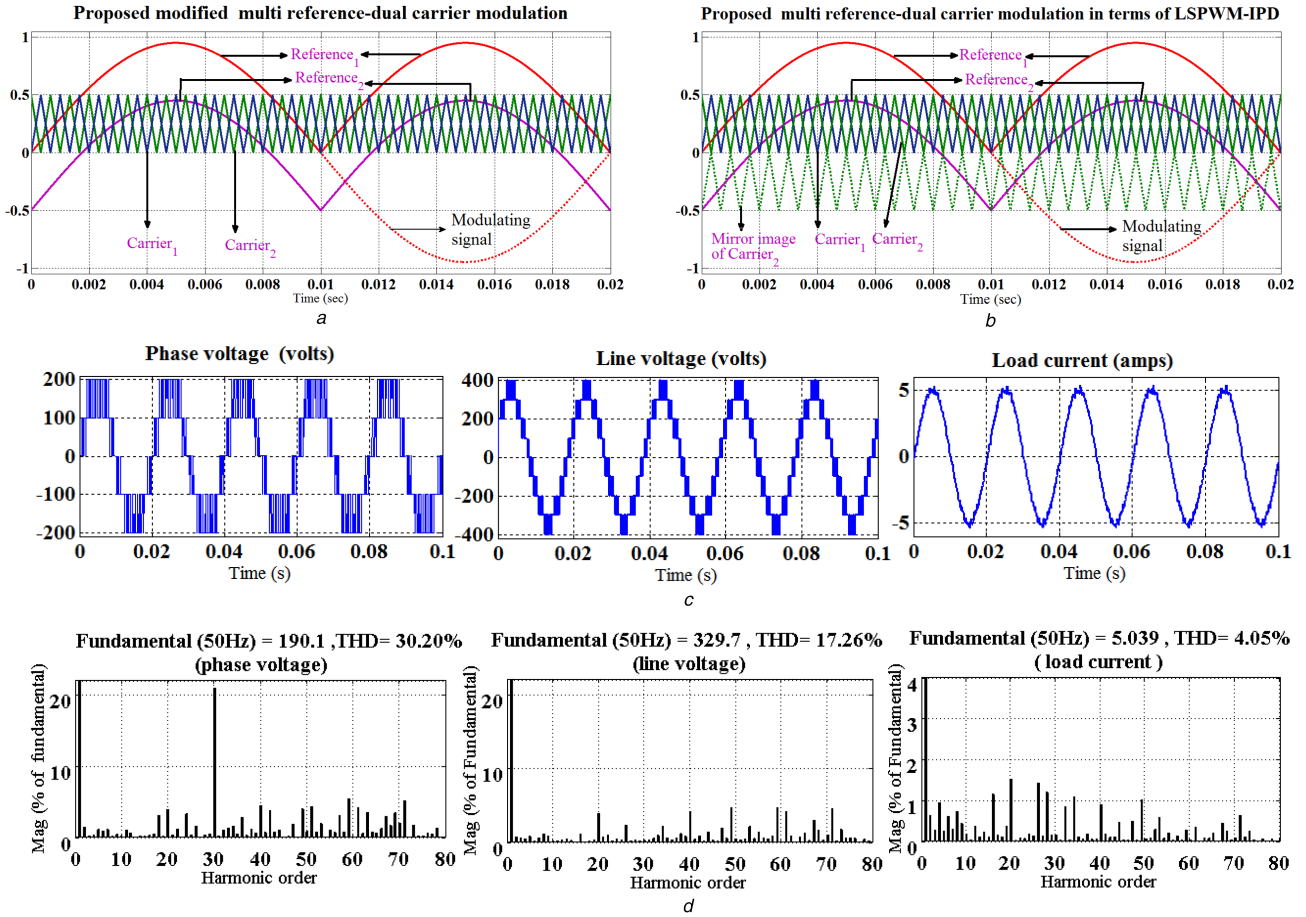**Fig. 4** *Modified multi-reference dual-carrier modulation scheme for a five-level T-type topology with $m_a = 0.95$ and $f_c = 1500$ Hz*
(a) Proposed scheme, *(b)* Carriers of proposed scheme in terms of LSPWM-IPD, *(c)* Phase voltage, line voltage and load current, *(d)* Respective harmonic spectra

$$m_f = \frac{f_c}{f_m} \qquad (6)$$

where V_m is the peak of the modulating signal, V_c is the peak of the carrier signal, f_c is the frequency of carrier signal, f_m is the frequency of the modulating signal and n is the levels in phase voltage.

Fig. 6*b* depicts a flowchart for the implementation of generalised switching logic for any number of levels. Here, 'i' indicates carrier number, 'n' is the number of levels in phase voltage, P_i is the switching pulse to obtain i^{th} level in phase voltage and S_i indicates the switching path for obtaining i^{th} level. Initially 'i' is assumed to be 1, and it varies from 1 to $(n-1)/2$. If the modified reference is greater than carrier$_{i\text{-min}}$ and less than carrier$_{i\text{-max}}$, then 'carrier$_i$' is compared with modified reference. This obtains a logic 'P_i' and it is high, if the modified reference is greater than 'carrier$_i$', else P_i is low. This pulse P_i is responsible for obtaining a voltage band of i to $(i-1)$, and polarity of this band is same as to polarity of the modulating signal. In this voltage band i to $i-1$, to obtain i^{th} level, pulse P_i is applied to the switching devices in S_i path and, to obtain $(i-1)$th level, pulse $(1 - P_i)$ is applied to the devices in S_{i-1} path. In case, if the modified reference is more than the carrier$_{i\text{-max}}$, then 'i' value is incremented by 1. In case if the modified reference turns less than carrier$_{i\text{-min}}$, then i is decremented by one. This logic continues as shown in Fig. 6*b*. It should be noted that, verifying maximum condition for carrier$_{(n-1)/2}$ should be avoided. Since, it is the carrier with peak magnitude, involving maximum condition to this carrier will limit the switching logic to under modulation.

Performance of this modified reduced carrier modulation scheme on a five-level T-type MLI for 2 kW, 0.9 PF load is shown in Fig. 7. Results are shown for $m_a = 0.95$ at 1500 Hz carrier

frequency. The phase voltage, line voltage and load current are shown in Fig. 7*a* and their corresponding harmonic spectra are shown in Fig. 7*b*. By comparing Figs. 7*a* and 4*c* it can be observed that the shape of phase and line voltage waveforms are identical. It can be further observed that the harmonic spectra in Figs. 7*b* and 4*d* are identical and verify the identical performance of this method with proposed multi-reference dual-carrier modulation scheme.

Finally comparative line THD performance of the conventional schemes (LSPWM-IPD, OPD and multi-reference) with the proposed and alternative carrier arrangement of proposed schemes with various modulation indices for a five-level MLI is shown in Fig. 7*c*. From this figure it can be concluded that the proposed modified multi-reference dual-carrier modulation and alternative carrier arrangement of the proposed schemes are identical to LSPWM-IPD. Fig. 7*c* also verifies the superior performance of proposed schemes over conventional modulation schemes.

4 Experimental results

To validate the performance of the proposed modulation schemes, a prototype of a five-level T-type topology is developed. The various components used for experimental set-up are given in Table 2. Control pulses for power circuit switching devices (IGBTs) are obtained from dPSACE-1104 R&D controller followed by driver circuit.

Initially, an experimental set-up of a five-level CHB is developed. To control the voltage, a various conventional LSPWM schemes are implemented to CHB inverter. Fig. 8 shows the experimental results obtained with conventional LSPWM techniques for $f_c = 1500$ Hz and $m_a = 0.95$. Fig. 8*a* shows the experimental results of phase and line voltage waveforms and their corresponding harmonic spectra with LSPWM-IPD technique. Similarly, Fig. 8*b* shows the experimental results of phase and line voltage waveforms and their corresponding harmonic spectra with LSPWM-OPD technique. The side-band harmonics of
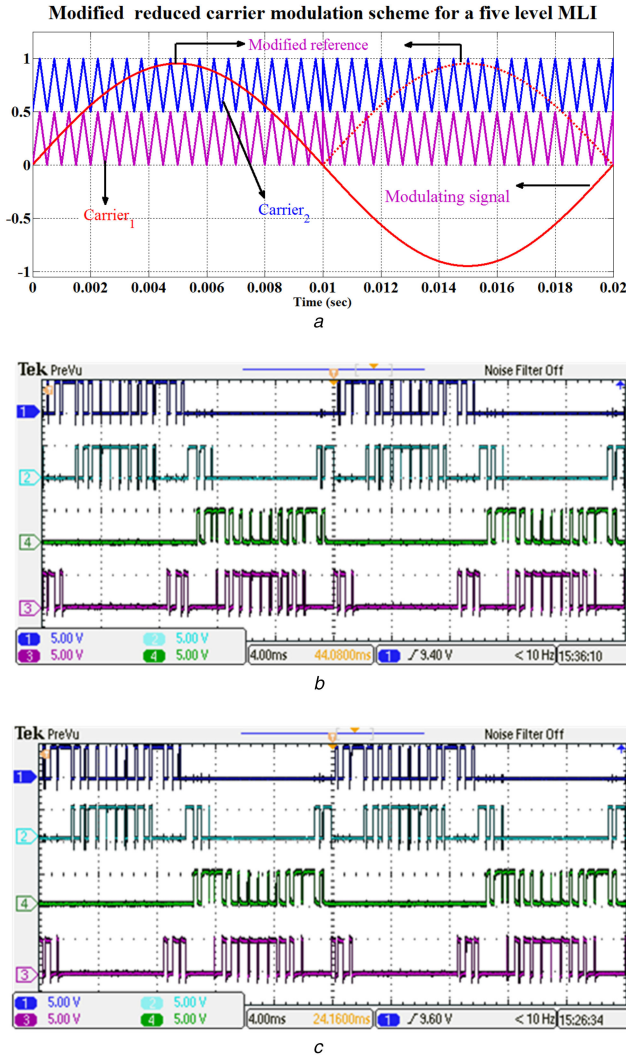
Fig. 5 *Five-level T-type MLI PWM*

(a) Carrier arrangement of reduced carrier scheme for five levels in phase, *(b)* Switching pulses of modified multi-reference dual-carrier modulation, *(c)* Switching pulses of modified reduced carrier modulation scheme. Trace 1: switching pulse to S_5; trace 2: switching pulse to S_1; trace 3: switching pulse to S_3; and trace 4: switching pulse to S_6

experimentally recorded harmonic spectra of Figs. 8*a* and *b* matches with literature [9]. This justifies the improved line THD performance of LSPWM-IPD (7.0%) over LSPWM-OPD (20.3%).

An experimental set-up of a five-level T-type MLI is developed, and its performance with conventional, proposed and alternative implementation of proposed scheme is evaluated. Fig. 9 shows the experimental results obtained with various modulation techniques for $f_c = 1500$ Hz and $m_a = 0.95$. Fig. 9*a* shows the experimental results of phase and line voltage waveforms and their corresponding harmonic spectra with conventional multi-reference modulation technique. Figs. 9*b* and *c* show the experimental results of phase and line voltage waveforms and their corresponding harmonic spectra with proposed modulation and alternate carrier arrangement of proposed multi-reference dual-carrier scheme, respectively.

From Figs. 9*a* and 8*b*, it is observed that phase and line THD of conventional multi-reference (23.3 and 20.3%) and LSPWM-OPD (23.4 and 20.3%). are similar. This is validated with simulation results too, where the phase and line THD performance of conventional multi-reference (29.4 and 25.4%) depicted in Fig 2*b* matches with LSPWM-OPD (29.4 and 25.4%) depicted in Fig. 3*d*. Comparison of Figs. 9*b* and *c* with Fig. 8*a* verifies that phase and line THD performance of the proposed multi-reference dual-carrier modulation scheme (23.2 and 7.3%) and modified reduced carrier modulation (23.3 and 7.1%) are identical to phase (23.3%) and line (7.0%) THD performance of LSPWM-IPD.
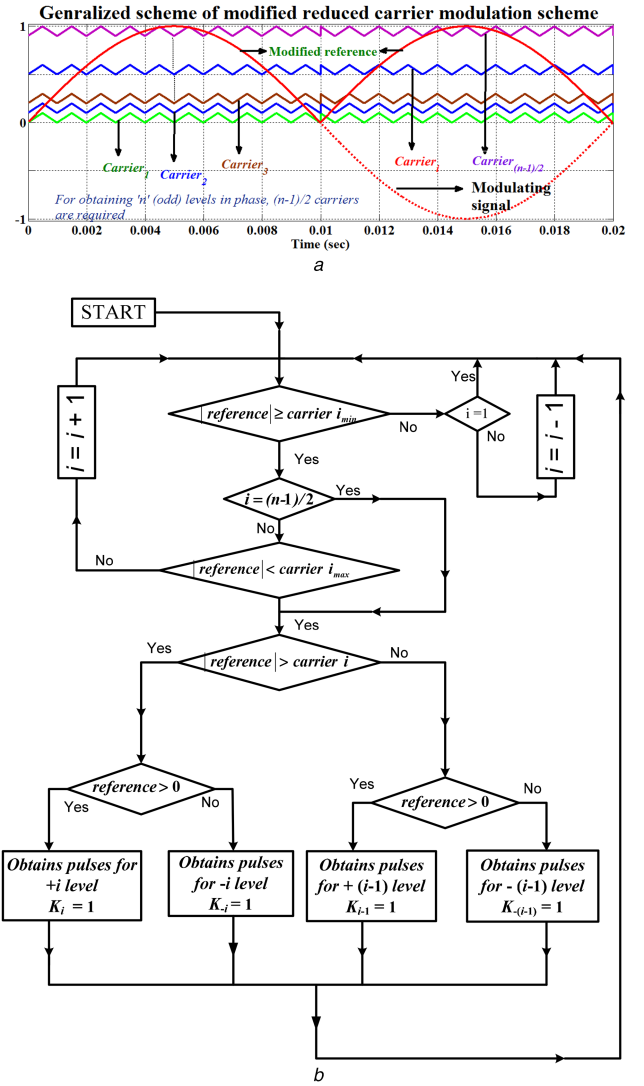

Fig. 6 *Generalisation of modified reduced carrier modulation scheme*
(a) Carrier arrangement, *(b)* Flowchart of its switching scheme

Finally, experimental line voltage THD performance of the conventional schemes (LSPWM-IPD, OPD and multi-reference) with the proposed and alternative carrier arrangement of proposed scheme with various modulation indices on a five-level MLI is shown in Fig. 9*d*. From this figure it can be concluded that the proposed multi-reference dual-carrier modulation and alternative carrier arrangement of the proposed schemes are identical to LSPWM-IPD. Fig. 9*d* also verifies the superior performance of proposed schemes over conventional modulation schemes. Fig. 9*d* is also in good agreement with Fig. 7*c* which is obtained with simulation.

However, there is a variation in THD recorded in simulation and experimental case (Figs. 7*c* and 9*d*). This is due to the MATLAB simulator, which measures the THD until Nyquist frequency (up to 499th order harmonics), where fluke meter used to measure experimental THD measures up to 49th order harmonics. However, minimising measurable THD frequency limit to 49th order in MATLAB simulator makes the simulation THD equal to experimental THD recorded. However, this is not opted in simulation because it is necessary to observe the complete harmonic spectrum of inverter output voltages.

5 Conclusion

In this paper, the poor harmonic performance of the conventional multi-reference modulation method for T-type MLI topology is analysed. To address this problem, a modified multi-reference dual-carrier modulation is proposed. The performance of the proposed modulation scheme is identical to LSPWM-IPD
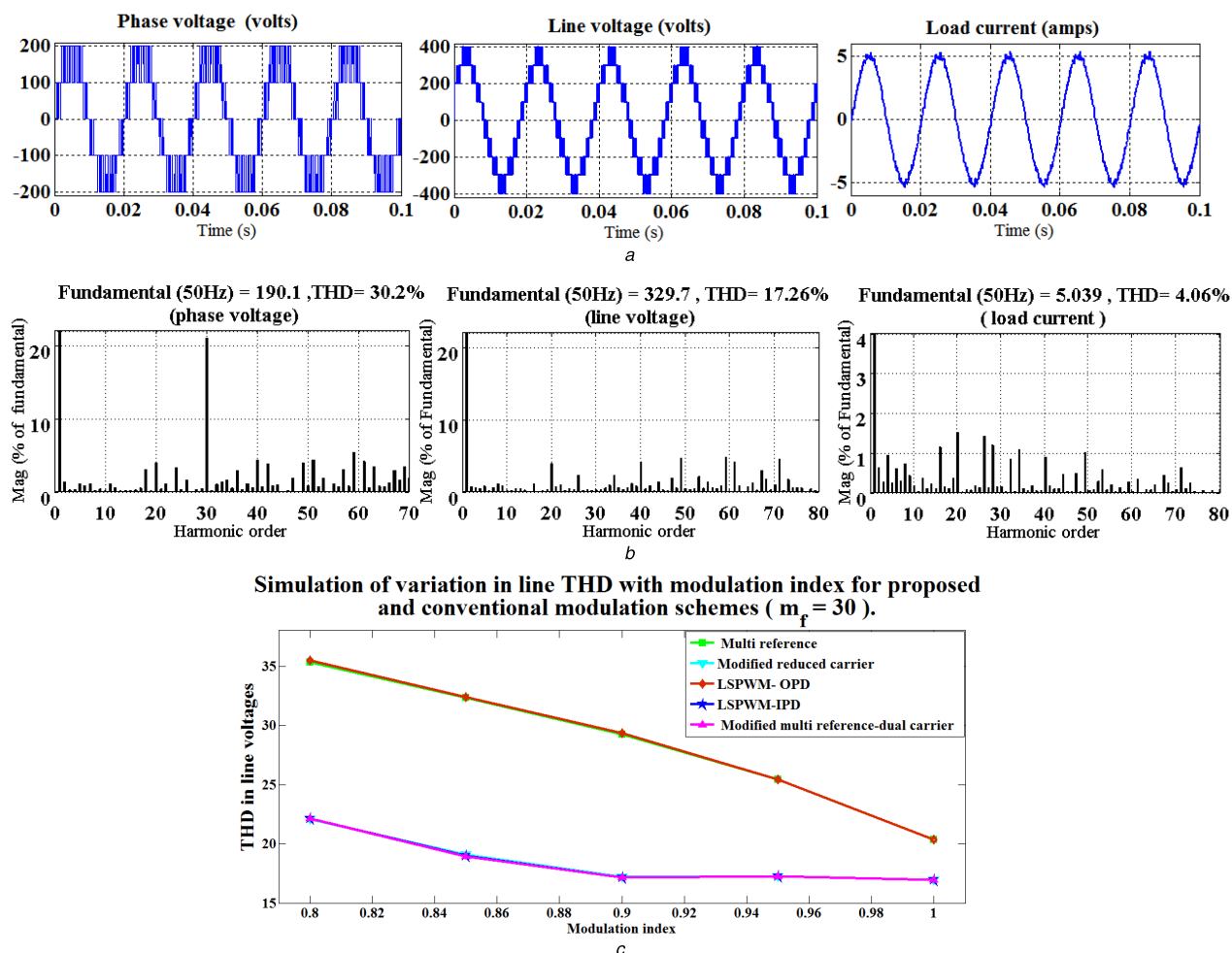
Fig. 7 *Performance of reduced carrier modulation on a five-level T-type MLI*
(a) Phase voltage, line voltage and load currents, *(b)* Respective harmonic spectra, *(c)* Simulink comparison of line THD among proposed and conventional schemes at various modulation indices

Table 2 Experimental parameters

Circuit	Component	Specification – type
100 V isolated dc power supplies	bridge rectifier (IC)	KBPC3510
	filter capacitor	450 V, 2250 µF.
	voltage regulator	LM5008
power circuit	switching device (IGBT) anti-parallel diode	XPT^{TM} −600 V - IXXH30N60B3 DPH 30 IS 600 HI
driver circuit	IC's	HEX 4010, IC 4081BC, HCPL 3120 / TLP 250
controller	dSPACE	DS1104 R&D controller board
	sampling time	50 µs
THD measurement	power quality analyser	fluke 435 series II

technique which is the best PWM technique with lowest THD value available. Further, to implement the proposed PWM scheme, an alternate carrier and modulation signals arrangement is also proposed which can be easily realisable on digital platforms. The performance of the proposed modulation schemes is evaluated with simulation and experimental studies on a five-level T-type MLI topology. The experimental studies are in good agreement with simulation studies and also verify the superior performance of the proposed schemes over conventional modulation schemes. A generalisation of the modified reduced carrier modulation to implement any number of levels for a T-type is presented with the help of a flowchart.
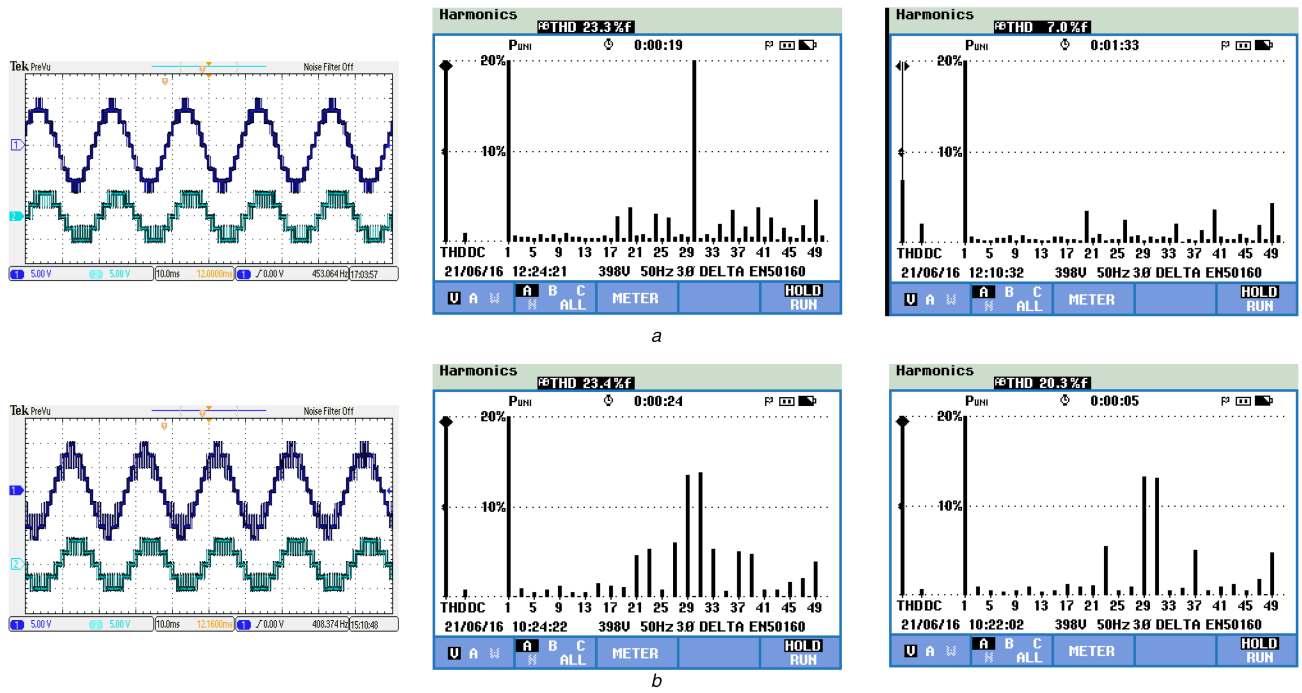
Fig. 8 *Experimental performance of LSPWM modulation scheme for a five-level CHB*
(a) Phase voltage and line voltage with its respective harmonic spectra of LSPWM-IPD scheme, *(b)* Phase and line voltages with its respective harmonic spectra of LSPWM-OPD scheme. (Scale: trace 1: line voltage, volts/div = 200 V, time/div = 10 ms and trace 2: phase voltage, volts/div = 200 V, time/div = 10 ms)
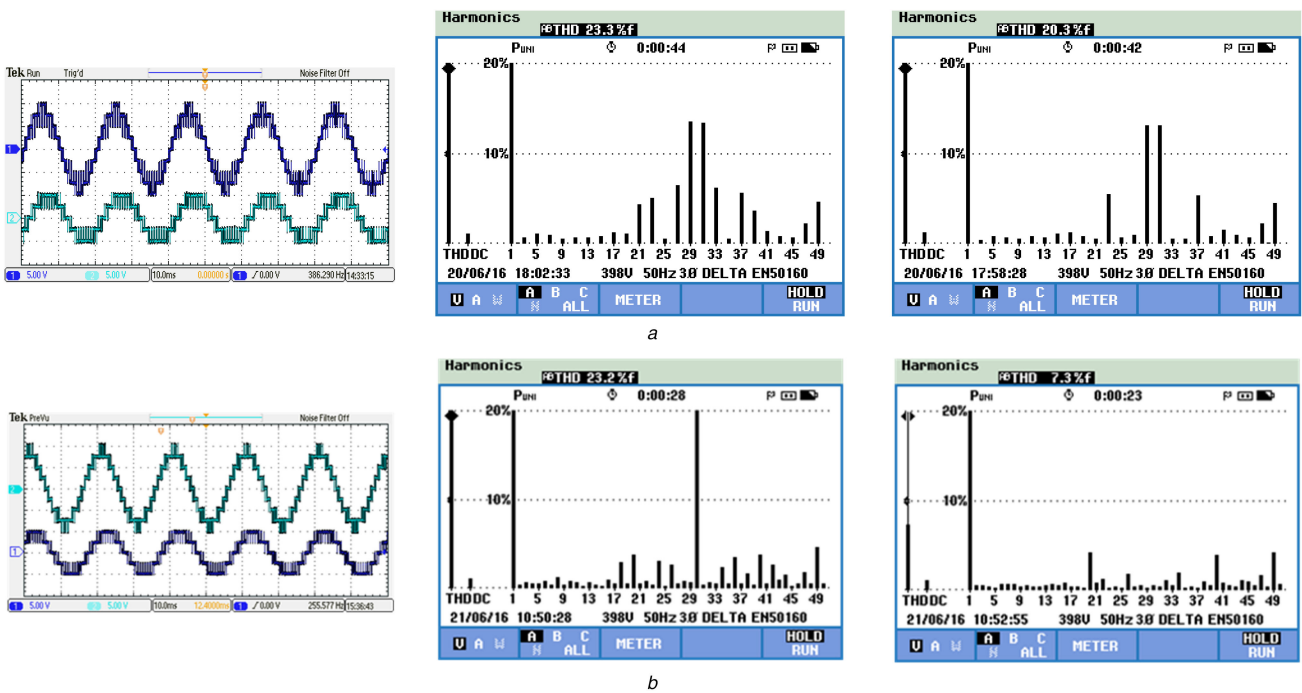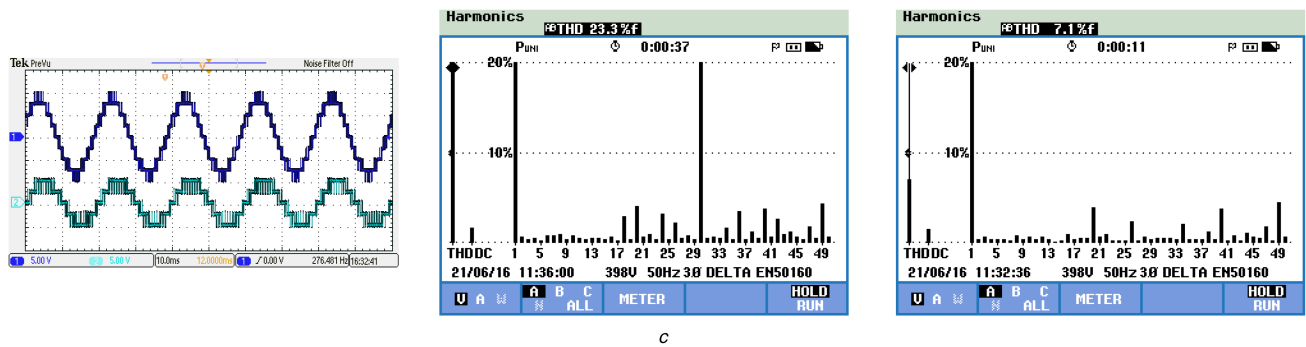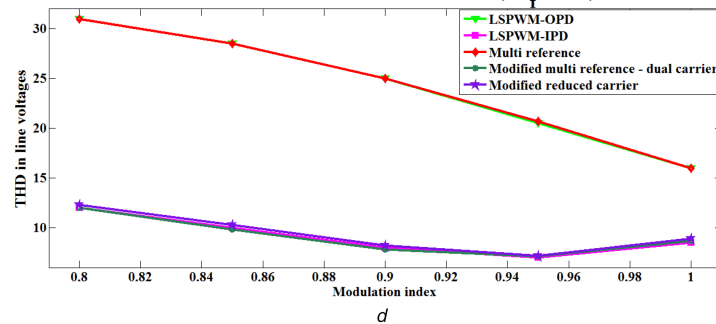

Fig. 9 *Continued*

c

d

Fig. 9 *Experimental performance of conventional and modified modulation schemes for a five-level T-type topology*

(a) Phase and line voltages with its respective harmonic spectra of conventional multi-reference modulation, *(b)* Phase and line voltages with its respective harmonic spectra of modified multi-reference dual-carrier modulation, *(c)* Phase and line voltages with its respective harmonic spectra of alternate carrier arrangement of proposed multi-reference dual-carrier scheme, *(d)* Experimental line THD comparison of proposed and conventional modulation schemes at various modulation indices for a five-level topology. (Scale: trace 1: line voltage, volts/div = 200 V, time/div = 10 ms and trace 2: phase voltage, volts/div = 200 V, time/div = 10 ms)

6 References

[1] Singh, B., Singh, B.N., Chandra, A.*, et al.*: 'A review of three-phase improved power quality AC–DC converters', *IEEE Trans. Ind. Electron.*, 2004, **51**, (3), pp. 641–660

[2] Franquelo, L.G., Rodriguez, J., Leon, J.I.*, et al.*: 'The age of multilevel converters arrives', *IEEE Ind. Electron. Mag.*, 2008, **2**, (2), pp. 28–39

[3] Kouro, S., Malinowski, M., Gopakumar, K., Pou, J., Franquelo, L.G., Wu, B., Rodriguez, J., Pérez, M.A., Leon, J.I.: 'Recent advances and industrial applications of multilevel converters', *IEEE Trans. Ind. Electron.*, 2010, **57**, (8), pp. 2553–2580

[4] Rodriguez, J., Lai, J.-S., Peng, F.Z.: 'Multilevel inverters: a survey of topologies, controls, and applications', *IEEE Trans. Ind. Electron.*, 2002, **49**, (4), pp. 724–738, doi: 10.1109/TIE.2002.801052

[5] McGrath, B.P., Holmes, D.G.: 'Multicarrier PWM strategies for multilevel inverters', *IEEE Trans. Ind. Electron.*, 2002, **49**, (4), pp. 858–867

[6] Sreenivasarao, D., Agarwal, P., Das, B.: 'Performance evaluation of carrier rotation strategy in level-shifted pulse-width modulation technique', *IET Power Electron.*, 2014, **7**, (3), pp. 667–680

[7] Dahidah, M.S.A., Agelidis, V.G.: 'Selective harmonic elimination PWM control for cascaded multilevel voltage source converters: a generalized formula', *IEEE Trans. Power Electron.*, 2008, **23**, (4), pp. 1620–1630

[8] Ahmed, I., Borghate, V.B.: 'Simplified space vector modulation technique for seven-level cascaded H-bridge inverter', *IET Power Electron.*, 2014, **7**, (3), pp. 604–613

[9] Carrara, G., Gardella, S., Marchesoni, M., Salutari, R., Sciutto, G.: 'A new multilevel PWM method: a theoretical analysis', *IEEE Trans. Power Electron.*, 1992, **7**, (3), pp. 497–505

[10] Gupta, K.K., Ranjan, A., Bhatnagar, P., Sahu, L.K., Jain, S.: 'Multilevel inverter topologies with reduced device count: a review', *IEEE Trans. Power Electron.*, 2016, **31**, (1), pp. 135–151

[11] Gupta, K.K., Jain, S.: 'Comprehensive review of a recently proposed multilevel inverter', *IET Power Electron.*, 2014, **7**, (3), pp. 467–479

[12] Ceglia, G., Guzman, V., Sanchez, C., Ibanez, F., Walter, J., Gimenez, M.I.: 'A new simplified multilevel inverter topology for DC–AC conversion', *IEEE Trans. Power Electron.*, 2006, **21**, (5), pp. 1311–1319

[13] Babaei, E., Laali, S., Bayat, Z.: 'A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches', *IEEE Trans. Ind. Electron.*, 2015, **62**, (2), pp. 922–929

[14] Gupta, K.K., Jain, S.: 'A novel multilevel inverter based on switched DC sources', *IEEE Trans. Ind. Electron.*, 2014, **61**, (7), pp. 3269–3278

[15] Park, S.-J., Kang, F.-S., Lee, M.H.*, et al.*: 'A new single-phase five-level PWM inverter employing a deadbeat control scheme', *IEEE Trans. Power Electron.*, 2003, **18**, (3), pp. 831–843

[16] Rahim, N.A., Chaniago, K., Selvaraj, J.: 'Single-phase seven-level grid connected inverter for photovoltaic system', *IEEE Trans. Ind. Electron.*, 2011, **58**, (6), pp. 2435–2444

[17] Odeh, C.I.: 'A cascaded multi-level inverter topology with improved modulation scheme', *Electr. Power Comp. Syst.*, **42**, (7), 2014, pp. 768–777, doi: 10.1080/15325008.2014.890974

[18] Rahim, N.A., Selvaraj, J.: 'Multistring five-level inverter with novel PWM control scheme for PV application', *IEEE Trans. Ind. Electron.*, 2010, **57**, (6), pp. 2111–2123

[19] Selvaraj, J., Rahim, N.A.: 'Multilevel inverter for grid-connected PV system employing digital PI controller', *IEEE Trans. Ind. Electron.*, 2009, **56**, (1), pp. 149–158

[20] Choi, J.S., Kang, F.S.: 'Seven-level PWM inverter employing series-connected capacitors paralleled to a single DC voltage source', *IEEE Trans. Ind. Electron.*, 2015, **62**, (6), pp. 3448–3459

[21] Najafi, E., Yatim, A.H.M.: 'Design and implementation of a new multilevel inverter topology', *IEEE Trans. Ind. Electron.*, 2012, **59**, (11), pp. 4148–4154

[22] Rahim, N.A., Elias, M.F.M., Hew, W.P.: 'Transistor-clamped H-bridge based cascaded multilevel inverter with new method of capacitor voltage balancing', *IEEE Trans. Ind. Electron.*, 2013, **60**, (8), pp. 2943–2956

[23] Samadaei, E., Gholamian, S.A., Sheikholeslami, A., Adabi, J.: 'An envelope type (E-type) module: asymmetric multilevel inverters with reduced components', *IEEE Trans. Ind. Electron.*, 2016, **36**, (11), pp. 7148–7156